IGBT Chip

Die In Wafer Form

650V
IC (nom) =20A
Vce(sat)typ=2.0V@IC(nom)@25℃
Fast IGBT
ShortCircuit Rated
150mm Wafer

Applications

- Motor Control Application
- Qualified For Industrial Market

Features

Non Punch Through (NPT) Technology
Low Vce(sat)
10μs Short Circuit Capability
Square RBSOA
Positive Vce(sat) Temperature Coefficient

Chip Type	Icn	Vce	Die size	Wafer size
SYC20PN65WK	20A	650V	4.45*4.32 mm^2	6 inch

Mechanical Parameters

Die size	4.45mm*4.32mm
Emitter pad size	See chip drawing
Gate pad size	2.02mm*0.82mm
Area total	19.22mm^2
Silicon thickness	100um
Wafer size	150mm
Maximum possible chips per wafer	709pcs
Passivation frontside	Polyimide
Pad metal	4000nm AlSiCu
Backside metal	Al - Ti - Ni/V - Ag, (1kA - 1kA - 2kA - 8kA) suitable for epoxy and soft solder die bonding
Die bond	Soft solder
Wire bond	Al, ≤500um
Reject ink dot size	∅ 0.65mm; max. 1.2mm
Storage environment (<6 months) for original and sealed MBB bags	Ambient atmosphere air, temperature 17°C – 25°C
Storage environment (<6 months) for open MBB bags	Acc. IEC 62258-3; Section 9.4 Storage Environment.

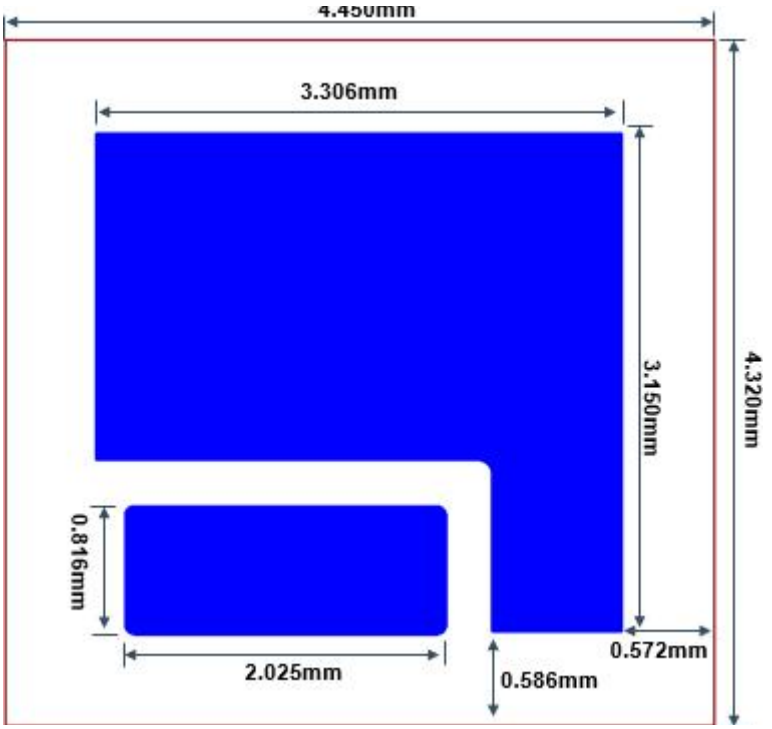
Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-emitter voltage, Tvj=25OC	VCE	650	V
DC collector current, limited by Tvj max 1	IC	20	A
Pulsed collector current, tp limited by Tvj max 2	IC,puls	40	A
Gate- emitter voltage	VGE	±20	V
Junction temperature	Tvj	150	C
Operating junction temperature	Tvj op	-40 - 125	C
Short circuit data 2 / 3 VGE=15V, VCC=600V, Tvj=150°C	tsc	10	μs

Static Characteristics (tested on chip)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Collector- emitter breakdown voltage	$V_{(BR)CES}$	V_{GE}=0V, I_C=250uA	650			V
Collector- emitter saturation voltage	$V_{CE(sat)}$	Ic=20A,V_{GE}=15V, T_{vj}= 25 C	1.7	2.0	2.3	V
Gate- emitter threshold voltage	$V_{GE(th)}$	V_{GE} =V_{CE}, I_C =250uA, T_{vj}= 25 C	4.3	4.8	5.3	V
Collector- emitter cut- off current	I_{CES}	V_{CE}=650V,V_{GE}=0V, T_{vj}= 25 C			20	uA
Gate- emitter leakage current	I_{GES}	V_{CE}=0, V_{GE}=20V, T_{vj}= 25 C			100	nA

1. Depending on thermal properties of assembly.
2. Not subject or production test - verified by design/characterization.
3. Allowed number of short circuits: <1000; time between short circuit


4.450mm
3.306mm
3.150mm
4.320mm
0.816mm
2.025mm
0.572mm
0.586mm

Bare Die Product Specifics

Test coverage at wafer level cannot cover all application conditions. Therefore it is recommended to test all characteristics which are relevant for the application at package level, including RBSOA and SCSOA.

Revision History

Revision	Subjects(major changes since last revision)	Date
1.0	Final date sheet	2021. 12. 13
1.1	Change specification name and company address	2022.10.27